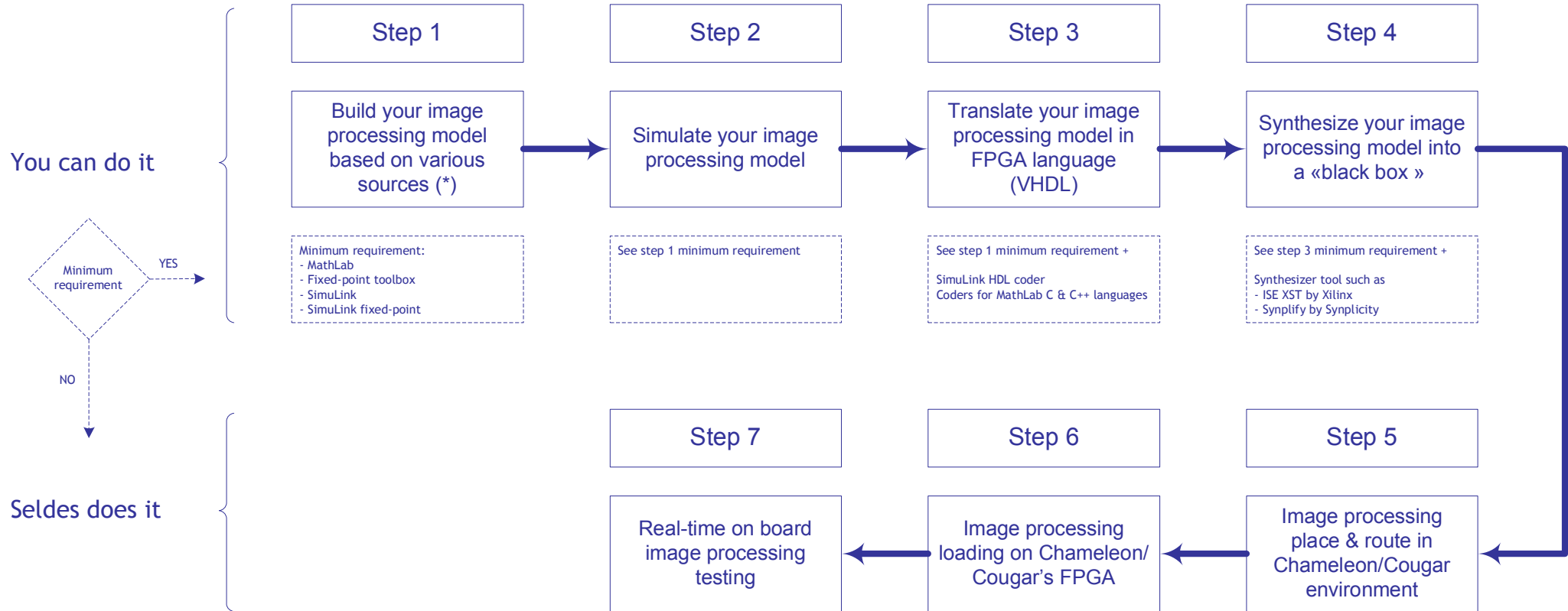


FPGA processing? DO IT YOURSELF !!

How to easily generate your real-time image processing under FPGA?
Partnership between SELDES and MathWorks



(*) Available sources for image processing model building:
(compatible with SimuLink HDL coder)

- Seldes blockset and hardware model for Chameleon/Cougar architecture
- MathWorks SimuLink BuiltIn block
- Xilinx blockset
- MathWorks Stateflow
- MathWorks Signal Processing blokset
- MathWorks Image Acquisition toolbox
- and much more coming !

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